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METHOD FOR PREVENTING POSTAMBL RINGING PHENOMENON IN DDR SDRAM

[DDR SDRAMeisoui Postambl Ringing Hyunsang Bangji Baeobeop]

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Specification

1. Title of the invention

Method for Preventing Postamble Ringing Phenomenon in DDR SDRAM

2. Brief description of the figures

Figure 1 is a timing chart for explaining a general postamble ringing phenomenon.

Figure 2 is a block diagram showing a general data input terminal being used to prevent an operation error due to the postamble ringing phenomenon.

Figure 3 is a block diagram showing a data input part of /2 the present invention for preventing the postamble ringing phenomenon in a memory device.

Figure 4 is a timing chart showing signals used.

[1] Numbers in the margin indicate pagination in the foreign text.

3. Detailed explanation of the invention

(Purpose of the invention)

(Technical field of the invention and prior art of the field)

The present invention pertains to a method for preventing a postamble ringing phenomenon in a memory device. In particular, the present invention pertains to a method for removing a phenomenon in which invalid data are written in a write operation in DDR SDRAM.

In general, in case a write operation is carried out in the DDR SDRAM, data are synchronized with a DQS signal being output from a memory controller and transmitted to an global input and output line in a memory device. On the other hand, if the memory controller transmits the DQS signal to the memory device, a postamble ringing phenomenon is sometimes caused, and in this case, the memory device can write invalid data, so that a wrong operation may be caused.

Next, referring to the figures, the ringing phenomenon being caused after the postamble is explained.

Figure 1 is a timing chart for explaining a general postamble ringing phenomenon. CLK is an external main clock being given to a DDR SDRAM, and a DQS signal is a signal being given from a memory controller. Data (DQ) are given to it by being synchronized with the rising edge or falling edge of the

DQS signal, and DQ are data being given to the memory device. Also, tDQSS is a time until the rising edge of the first DQS signal is generated after a write command is given, and tDQSS is generally determined as 0.75-1.25 tCK. Here, tCK is a period of an external main clock (CLK). For reference, in Figure 1, the data (DQ) being sequentially are indicated by 1, 2, 3, and 4, and 5 and 6 mean invalid data that may be given by the ringing phenomenon.

In a general write operation, the data (1, 2) being input by being synchronized with the rising edge and the falling edge of the first DQS signal are synchronized with A time of the external main clock (CLK) and transmitted to the input terminal of an input and output sensing amplifier. Also, the data (3, 4) being input by being synchronized with the rising edge and the falling edge of the second DQS signal are synchronized with B time of the external main clock (CLK) and transmitted to the input terminal of an input and output sensing amplifier.

On the other hand, as shown in the figure, in case the ringing phenomenon (that is, an unstable transition state of the DQS signal) is caused after a write postamble, a DQS buffer for receiving the DQS signal is decided as a valid DQS. For this reason, invalid voltage levels (5, 6) on the DQ, which are synchronized with the rising and falling edge of the DQS signal

generated by the ringing phenomenon, replace the valid data (3, 4) stored in a data input latch. Therefore, the invalid data (5, 6) are synchronized with B time of the external main block (CLK) and transmitted to the input terminal of the data input and output sensing amplifier, causing an error.

Figure 2 is a block diagram showing a general data input terminal being used to prevent an operation error due to the postamble ringing phenomenon.

As shown in Figure 2, in the prior art, in case the falling edge of the last DQS signal (meaning the falling edge of the second DQS signal) being output from the DQS latch is generated, an operation error due to the ringing phenomenon is prevented by disabling the DQS latch by using a DQS latch control part (dis_dsb).

However, in such a conventional method, a stable write operation is difficult under the condition in which tDQSS is 0.75-1.25 tCK. The reason for this is that in a DQS falling signal, after receiving it as an input, the buffer should be disabled and the buffer should be set to a standby state for the input of the next DQS falling signal. However, it is impossible to control the timing for it, and at a time of a high-speed operation, an input signal cannot completely overcome a wide range of ringing phenomenon being generated after 0.75-1.25 tCK.

Also, in case only the falling signal of the DQS buffer is controlled, a timing mismatch is caused at the rising and falling of the DQS signal, compared wit the external main clock (CLK). In this case, since the rising and falling timing of the DQS signal is identically controlled, compared with the external main clock (CLK) in accordance with the PVT (Process, Voltage, and Temperature) change, the conventional method is difficult to be applied to the memory device of a high-speed operation. /3

(Technical problems to be solved by the invention)

The present invention has been proposed to solve the above-mentioned problems, and its purpose is to provide a method for preventing a postamble ringing phenomenon in a memory device that enables a stable write operation under the condition in which tDQSS is 0.75-1.25 tCK.

(Constitution and operation of the invention)

The method for preventing a postamble ringing phenomenon in a DDR SDRAM of the present invention consists of (a) a step that receives a DQS signal through a DQS buffer and receives several data through a data input buffer; (b) a step that stores the above-mentioned DQS signal being output from the above-mentioned DQS buffer in a DQS latch; (c) a step that is generates a first signal by being synchronized with the rising edge of the above-mentioned DQS signal and generates a second signal by being

synchronized with the falling edge of the above-mentioned DQS signal; (d) a step that stores the first data of the above-mentioned several data being output from the above-mentioned data input buffer by being synchronized with the rising edge of the above-mentioned first signal; (e) a step that stores the second data of the above-mentioned several data being output from the above-mentioned data input buffer by being synchronized with the rising edge of the above-mentioned second signal; and (f) a step that transmits the above-mentioned first and second data stored in the above-mentioned data input latch by being synchronized with the falling edge of the above-mentioned second signal. (g) The operation of the above-mentioned DQS latch is controlled using a control signal being generated by being synchronized with the rising edge of the above-mentioned first signal at the above-mentioned step (d).

In the present invention, the operation of the above-mentioned DQS latch is cut off while the above-mentioned control signal maintains the enable state at high level.

In the present invention, the above-mentioned control signal is disabled by a data input strobe pulse signal for enabling the above-mentioned input sensing amplifier.

In the present invention, a ringing phenomenon cut-off part, which generates the above-mentioned control signal by

being synchronized with the rising edge of the above-mentioned first signal can control the enable section of the above-mentioned control signal by controlling its delay time.

(Application example)

Next, referring to the figures, an application example of the present invention is explained in further detail.

Figure 3 is a block diagram showing a data input part of the present invention for preventing the postamble ringing phenomenon in a memory device.

In Figure 3, a DQS buffer (300) is a device that receives and buffers a DQS signal, and a DQS latch (310) receives and latches a signal output from the DQS buffer (300).

A Din buffer (320) as a data input buffer receives and buffers data (DQ), and a Din latch (330) as a data input latch receives and latches a signal output from the Din buffer (320).

A Din IOSA (350) as a data input and output sensing amplifier receives data being output from the Din latch (330) as a data input buffer, amplifies them, and transmit the amplified data to a global input and output line.

Finally, if a rising edge of the DQS signal being output from the DQS latch is generated, a ringing phenomenon cut-off part (340) as a characteristic part of the present invention

receives its inverted signal and outputs a signal (dis_dqs) for controlling the operation of the Din latch (330).

Next, the operation of the circuit shown in Figure 3 is explained.

In a write operation, data (DQ: for example, data 1 and 2 in Figure 1) are stored in the Din latch (330) with the rising edge and the falling edge of the first DQS signal being input from the outside are stored.

The data (DQ) stored in the Din latch (330) are aligned by being synchronized with the falling edge of the DQS signal being output from the DQS latch (310) and given to the Din IOSA (350). Here, the data that are aligned by being synchronized with the falling edge of the DQS signal being output from the DQS latch (310) and given to the Din IOSA (350) are indicated by algn_f.

Next, the data stored in the Din IOSA (350) are /4 transmitted to a global input and output line by a data in strobe pulse signal (dinstbp) for enabling the operation of the Din IOSA (350).

The above-mentioned operation is applied in the same manner to the data (DQ: for example, data 3 and 4 in Figure 1) to the Din latch (330) by being synchronized with the rising edge and the falling edge of the second DQS signal.

For reference, a first signal and a second signal (dsrt2, dsft2) are generated. The first signal is generated by being synchronized with the rising time of the DQS signal, and the second signal is generated by being synchronized with the falling time of the DQS signal. Then, the data input into the data input latch are synchronized with the rising edge of the first signal and the second signal, and each data is latched and transmitted to the data input sensing amplifier at the falling time of the second signal.

On the other hand, as explained above in the prior art, if the ringing phenomenon is caused after the postamble, the data (3,4) stored and aligned in the Din latch (330) synchronized with the falling edge of the last DQS signal (for example, the second DQS signal of Figure 1) are sometimes replaced with wrong data (5 and 6 of Figure 1) by being synchronized with the rising and falling edge of a wrong DQS signal generated by the ringing phenomenon.

In order to cut off this ringing phenomenon, the present invention provides the ringing phenomenon cut-off part (340) as shown in Figure 3.

If the rising edge of the DQS signal being output from the DQS latch is generated, the ringing phenomenon cut-off part

(340) receives its inverted signal and outputs a control signal (dis_dqs) for cutting off the operation of the DQS latch (320).

Then, the ringing phenomenon cut-off part (340) releases the cut-off of the DQS latch so that new data can be applied to the Din latch (330) by a data in strobe pulse signal (dinstbp) or another timing signal (for example, clkp4) with a waveform having the same period.

In other words, in the present invention, since the signal (dis_dsb) for controlling the DQS latch is generated by being synchronized with the signal (dsr2: the signal being output by being synchronized with the rising edge of the DQS signal) being output from the DQS latch, the DQS latch can be controlled prior to the conventional case in terms of time. In this case, it can be understood that the time margin is larger than that of the conventional case where the operation of the DQS latch is controlled by being synchronized with the dsft2 (dsf2: the signal being output by being synchronized with the falling signal of the DQS signal). In this case, as can be seen from Figure 4, it can be understood that the operation of the DQS latch is cut off for a defense section and the DQS ringing generation is also effectively cut off. The defense section is released by the ringing phenomenon cut-off part (340) as mentioned above. In other words, the DQS latch is controlled so

that new data can be given to the Din latch (330) by the data in strobe pulse signal (dinstbp) or another timing signal (for example, clkp4) with a waveform having the same period.

Next, referring to Figures 4a and 4b showing timing charts of the signals used in Figure 3, the method for preventing the postamble ringing phenomenon of the present invention is explained. For reference, the waveform diagram of Figure 4a shows the method for preventing the preamble ringing phenomenon when tDQSS is 0.75 tCK, and the waveform diagram of Figure 4b shows the method for preventing the preamble ringing phenomenon when tDQSS is 1.25 tCK.

As can be seen from Figure 4a, the control signal (dis_dqs) being output from the ringing phenomenon cut-off part (340) is enabled at high level by the dsrt2 signal. The high-level section (enable section) of the control signal (dis_dqs) is a defense section. The low-level section (disable section) of the control signal (dis_dqs) is a reset section and enables a normal operation of the DQS latch (320). As shown in the figure, it can be understood that if a ringing phenomenon is caused in the DQS signal, since the control signal (dis_dqs) maintains an enable state, the operation of the DQS latch (320) is cut off, so that the ringing is prevented.

The case of Figure 4b for explaining the method for preventing the postamble ringing phenomenon when tDQSS is 1.25 tCK is actually the same as the case of Figure 4a, and clkp4 shows a signal with the same timing clock as that of the dinstbp signal. For reference, as can be seen from Figure 3, the data stored in the Din IOSA at the rising edge of the dinstbp signal (that is, clkp4 signal in Figure 4) are transmitted to the global input and output line. For reference, in Figures 4a and 4b, the width of the defense section can be controlled by controlling the delay time in the ringing phenomenon cut-off part (340).

As mentioned above, in the method for preventing the postamble ringing phenomenon in the memory device of the present invention, if valid data are stored and aligned in the data input latch, the above-mentioned aligned data are prevented from being replaced by the ringing phenomenon cut-off part, the above-mentioned data are transmitted to the global input and output line by the data in strobe pulse signal, and the above-mentioned data input latch can normally receive the next data (new data). In other words, in order to prevent invalid data from being written in memory cells due to the postamble ringing phenomenon during a write operation, the data in strobe pulse signal is used, and the data stored in the data input latch are

maintained for a fixed time before the data in strobe pulse signal is given. Also, the party concerned can sufficiently predict that the technical concept of the present invention can be applied in the same manner in addition general DDR SDRAM. /5

(Effects of the invention)

As can be seen from the above, in case a circuit for preventing a wrong operation due to the postamble ringing phenomenon by the method of the present invention, a write operation can be stably carried out even in a high-speed operation with a data rate of 400 MHz, and as can be seen in Figures 4a and 4b, a stable write operation can also be carried out under the condition in which tDQSS is 0.75-1.25 tCK.

4. Claims

1. A method for preventing a postamble ringing phenomenon in a DDR SDRAM, characterized by the fact that in a method for a postamble ringing phenomenon in a DDR SDRAM, it consists of (a) a step that receives a DQS signal through a DQS buffer and receives several data through a data input buffer; (b) a step that stores the above-mentioned DQS signal being output from the above-mentioned DQS buffer in a DQS latch; (c) a step that is generates a first signal by being synchronized with the rising edge of the above-mentioned DQS signal and generates a second

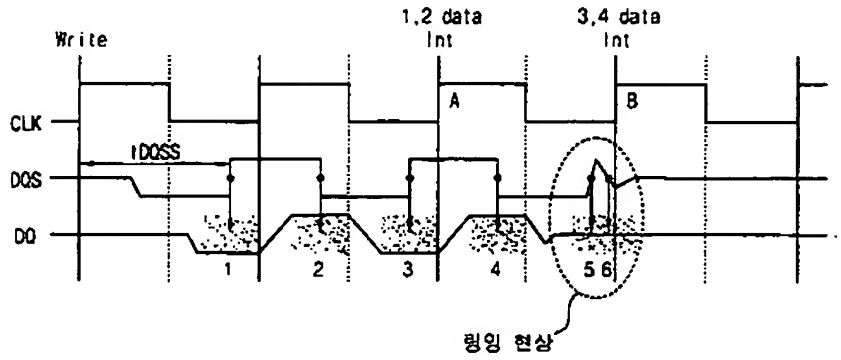
signal by being synchronized with the falling edge of the above-mentioned DQS signal; (d) a step that stores the first data of the above-mentioned several data being output from the above-mentioned data input buffer by being synchronized with the rising edge of the above-mentioned first signal; (e) a step that stores the second data of the above-mentioned several data being output from the above-mentioned data input buffer by being synchronized with the rising edge of the above-mentioned second signal; and (f) a step that transmits the above-mentioned first and second data stored in the above-mentioned data input latch by being synchronized with the falling edge of the above-mentioned second signal; and (g) the operation of the above-mentioned DQS latch is controlled using a control signal being generated by being synchronized with the rising edge of the above-mentioned first signal at the above-mentioned step (d).

2. The method for preventing a postamble ringing phenomenon in a DDR SDRAM of Claim 1, characterized by the fact that the operation of the above-mentioned DQS latch is cut off while the above-mentioned control signal maintains the enable state at high level.

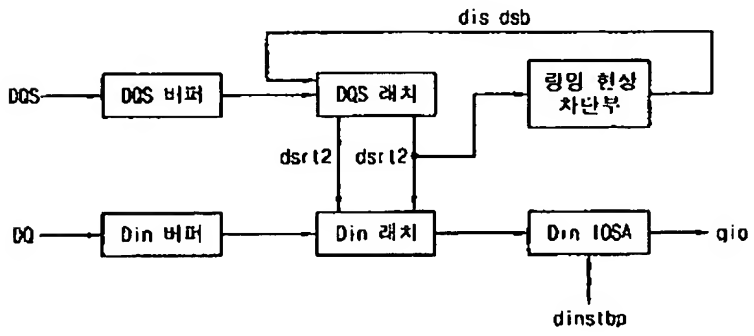
3. The method for preventing a postamble ringing phenomenon in a DDR SDRAM of Claim 2, characterized by the fact

that the above-mentioned control signal is disabled by a data input strobe pulse signal for enabling the above-mentioned input sensing amplifier.

4. The method for preventing a postamble ringing phenomenon in a DDR SDRAM of Claim 1, characterized by the fact that a ringing phenomenon cut-off part, which generates the above-mentioned control signal by being synchronized with the rising edge of the above-mentioned first signal can control the enable section of the above-mentioned control signal by controlling its delay time.



도면2



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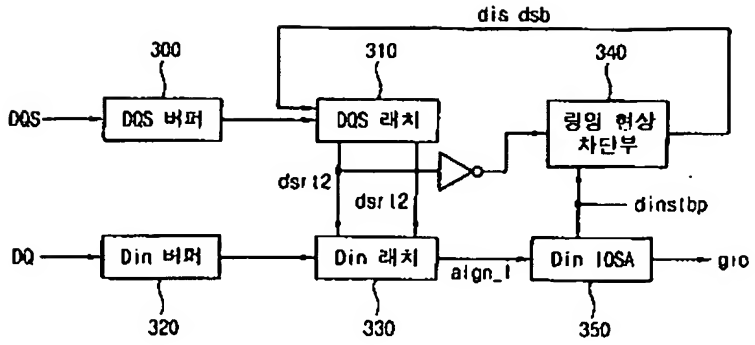

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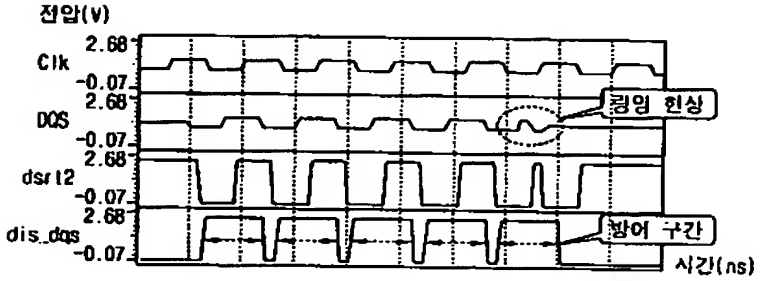

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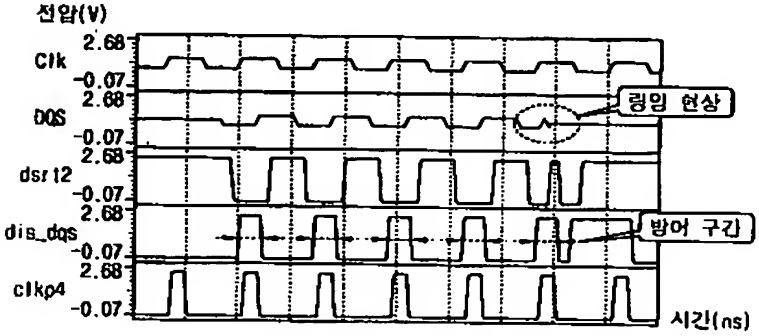

Figure 1:

1. Ringing phenomenon

Figure 2:

1. DOS buffer

2. DOS latch

3. Ringing phenomenon cut-off part

4. Din Buffer

5. Din latch

Figure 3:

300 DOS buffer

310 DOS latch

320 Din buffer

330 Din latch

340 Ringing phenomenon cut-off part

Figure 4:

1. Voltage (V)

2. Ringing phenomenon

3. Defense section

4. Time (ns)